Design, fabrication and Characterization of High Speed detector for future 100 Gbit/s access network

Risab GNANAMANI[1,2], Cristell MANEUX[1], Marina DENG[1], Chhandak MUKHERJEE[1] and Christophe CAILLAUD[2]

[1] IMS Laboratory, University of Bordeaux, UMR CNRS 5218, 33405 Talence, France
[2] III-V Lab, A Joint Lab between Nokia Bell Labs, Thales Research & Technology and CEA-LETI, 91767 Palaiseau, France
* risab.gnanamani@3-5lab.fr

Emergence of new applications like cloud computing, video on demand or deployment of high-speed cellular network lead to an increasing demand of high-speed short reach transmission for access network or data centre. Due to the low sensitivity of PIN receiver and the lack of APD above 25 Gb/s, optical pre-amplification is a promising concept for high-speed receiver.

For the photonic integrated circuit (PIC) a pre-amplification section (SOA) is connected to a high-speed detector (PIN photodiode), which forms the SOA-PIN receiver. The aim of the thesis is to design, fabricate and characterize a high-speed detector for 100 Gbit/s access network.

From the knowledge obtained from bibliography of previous works, we use UTC (Uni-Travelling Carrier) as photodiode for higher speed. For optimal performances, gain section (laser, amplifier) should be in buried structure (lower optical losses, better thermal dissipation) whereas high-speed section (modulator, photodiode) should be in deep ridge structure to lower device capacitance.

From the S-parameter measurements of UTC-PD, capacitance analysis was being carried out by doing equivalent circuit extraction. This work extends the device's compact modelling. Compact modelling helps to understand and model the device for future optimization and insertion into photonic integrated circuit.

With the detailed learning of existing fabrication process and design methodology by participating in the fabrication process, possible optimization to the new design is proposed with the help of simulations.

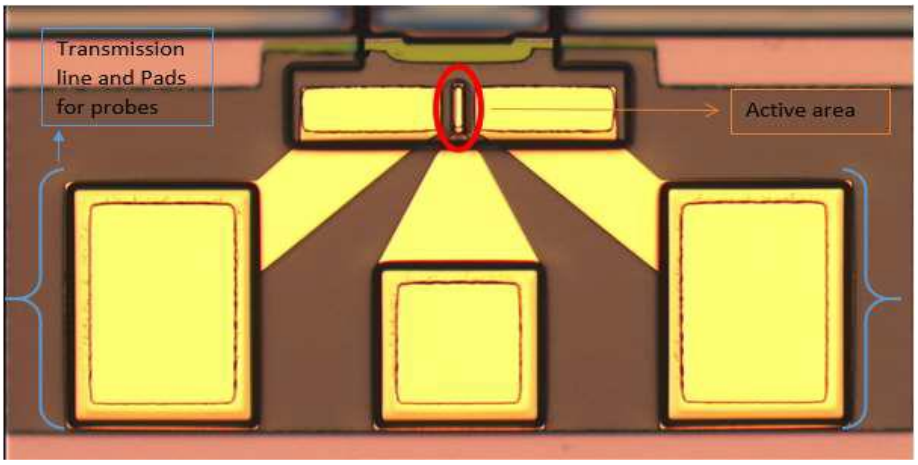

Figure 1 Photograph of UTC-PD